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A Comprehensive Study on Low Power VLSI Design Strategies

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***Abstract* – The rise in battery-powered electronic devices has led to an increase in the use of CMOS circuits. These circuits are crucial for development, and as the chip size decreases, power consumption also decreases. Therefore, it is important to optimize and design these circuits accordingly. This paper explores various power dissipation and optimization techniques, providing guidance to designers in achieving the optimal balance between performance and optimization.**

***Keywords* – Power dissipation, Static power dissipation, Dynamic power dissipation, Transistor stacking, clock gating.**

I. INTRODUCTION

Over the past few decades, there has been a significant rise in the production and demand for silicon chips, which are utilized in a wide range of industries, including healthcare and computing. The VLSI industry can be categorized into two main types: BJT based and MOSFET based. Notably, the size of these chips has considerably decreased from 90nm to 7nm in recent times. Previously, designers primarily prioritized areas such as performance, design, and cost. However, in recent years, there has been a shift towards placing greater emphasis on power consumption, dissipation, and the utilization of low power components. The primary objective for chip designers is to achieve maximum performance with minimal power, considering the reduced size of the chips. By minimizing power dissipation, we can also reduce the costs associated with packaging and cooling techniques. Additionally, due to the growing number of battery-powered devices like smartphones and laptops, developers are increasingly focused on optimizing power consumption. This paper will primarily delve into the various causes and types of power dissipation, low power design techniques, and power management strategies.

Power dissipation can occur in various ways and is generally categorized into two types Static power dissipation and Dynamic power dissipation

The total power dissipated in any circuit is given by the term, P total =P dynamic + P static + P short circuit

The primary distinction between static and dynamic power dissipation lies in their occurrence. Static power dissipation takes place when the circuit is not in use, whereas dynamic power dissipation occurs when the circuit is actively transitioning between different states. Additionally, power may be consumed during the charging and discharging operations.

1. DYNAMIC POWER DISSIPATION

Where,

α = Switching factor, C = Load capacitance

$$P_{Total} = \alpha f * C * V_{dd}^2 + f * I_{short} * V_{dd} + I_{leak} * V_{dd}$$

V_{dd} = Voltage

f = Clock frequency

I_{short} = Short circuit current

I_{leak} = Leakage current

There are two additional types of dynamic power loss, namely short circuit and switched power dissipation, which are influenced by factors such as voltage, capacitance, and frequency. Lowering the value of V_{dd} can decrease power dissipation, but it may also result in a decline in performance.

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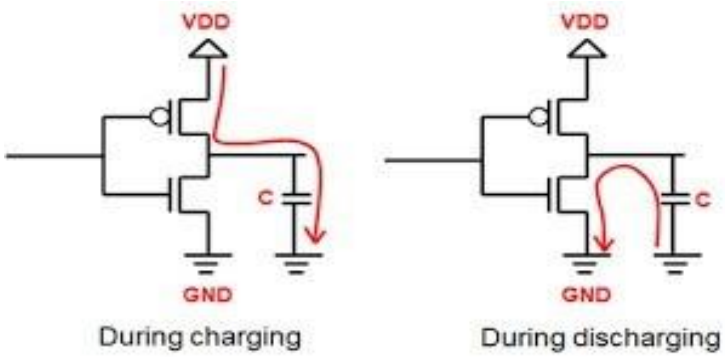

Fig. 1: Dynamic power dissipation

2. POWER DISSIPATION IN SWITCHING

Within CMOS circuits, a significant number of capacitors and parasitic elements contribute to the overall gate capacitance. These circuits consist of two networks: the Pull up network, which is composed of pMOS transistors, and the Pull down network, which is made up of nMOS transistors. During different operations, the capacitors undergo charging and discharging processes. The charging process takes place through the P-type devices in the Pull up network, while the discharging process occurs through the Pull down network.

3. SHORT CIRCUIT POWER DISSIPATION

When the input voltage (V_{dd}) exceeds the threshold voltage, the NMOS is considered to be in the ON state, while the pMOS is in the OFF state, resulting in power dissipation due to short circuit. Conversely, if the input voltage is lower than the threshold voltage (V_{dd} - V_{in}) in the pMOS, the opposite occurs. During a brief period of time, when the input voltage fluctuates between the values of V_{dd} and ($V_{dd} - V_{th}$), both the nMOS and pMOS are in the ON state.

The Short circuit power dissipation is represented by the term:

$$P_{Short\ circuit} = \beta/12 * (V_{dd} - 2V_{th})^3 * \tau/T_p$$

4. GLITCHING

The primary cause of the glitching power dissipation is a combination of switching and short circuit dissipation. This phenomenon is mainly attributed to the glitches that typically manifest at the output, which heavily rely on the gates utilized, logic, and function. These glitches result in the dissipation of short circuit power when there is a transition of state, and the voltage reaches alarmingly high levels. However, this issue can be mitigated by adjusting the input and threshold voltage.

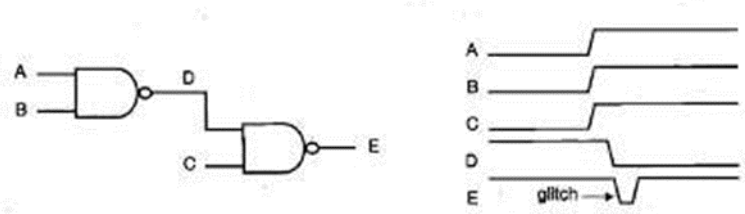

Fig. 2: Output Showing glitch

5. STATIC POWER DISSIPATION

Static power dissipation, also known as leakage power, occurs when the circuit is not in use. It occurs when the voltage is increased and the transistor enters the sub-threshold state, resulting in reverse current flow from the oxide to the P-N junction, causing leakage power. This occurrence can be managed through the implementation of multiple threshold voltages, body bias, and transistor stacking.

II. POWER MANAGEMENT TECHNIQUES

There are several methods available to implement power management in a CMOS circuit through design modifications:

❖ STATIC POWER OPTIMIZATION

1. Multiple threshold voltage (V_{th})

This approach aims to reduce leakage and standby power dissipation in CMOS circuits by utilizing different levels of threshold voltage for different circuit states. By setting a high threshold voltage, leakage current can be minimized, while a low threshold voltage is used during operation mode to achieve high performance. This technique also helps eliminate glitches in the circuit.

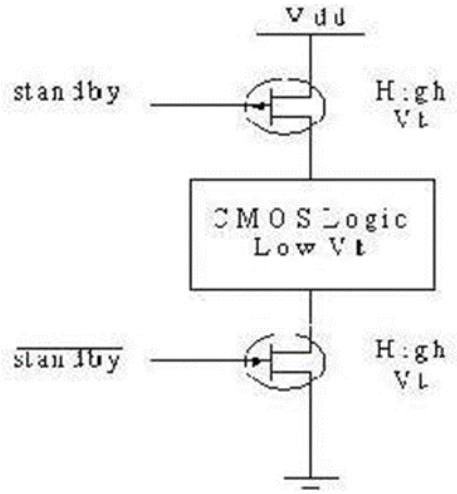

Fig. 3: CMOS Circuit

2. Body biasing technique

It is a method used to connect transistors to a bias instead of directly connecting them to the source voltage or ground. The purpose of this technique is to create a strong inversion at the channel and prevent any leakage of drain current during transmission. To achieve low leakage currents, reverse body biasing is applied between the drain and body.

3. Transistor stacking

on the other hand, involves connecting two transistors in series while they are in the off state. This technique significantly reduces power leakage compared to using a single transistor in the off position. The effectiveness of transistor stacking depends on the source voltage, as an increase in the source voltage leads to a decrease in the subthreshold current.

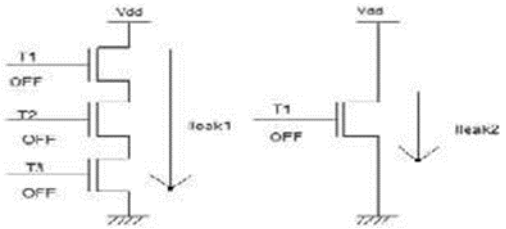

Fig. 4: Transistor Stacking

4. Lector approach

The LECTOR method is employed to manage the leakage current in CMOS circuits while keeping the dynamic power dissipation at a minimum. The circuit consists of two transistors: a leakage control transistor and a transistor whose source controls the gate of the other transistor. This arrangement effectively increases resistance from the ground, resulting in reduced leakage. The LECTOR technique is effective in both the active and non-active states of the transistor.

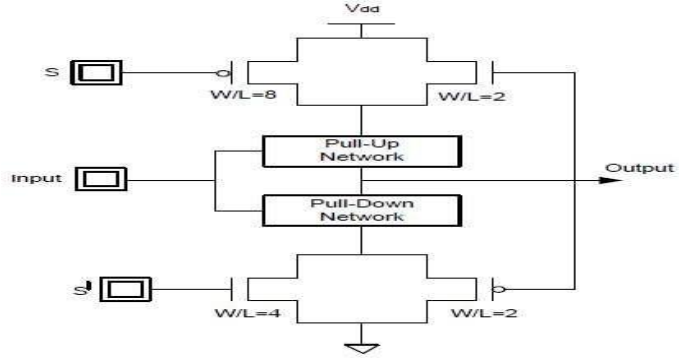

Fig. 5: Lector Technique

❖ **DYNAMIC POWER OPTIMIZATION**

1. Multiple source voltage (V_{dd})

The advantage of having multiple source voltage is that, it is useful in eliminating both static and dynamic power dissipation. There are different supply voltages for different modes, the high performance modes get high V_{dd} and the low performance mode is assigned with low supply voltage. Thus it is used for deriving high performance and also to reduce power dissipation.

2. Dynamic voltage and frequency scaling

The circuits require different power for handling different types of activities, so on decreasing the clock frequency there is a decrease in the source voltage and can be used to save power, the main advantage of this technique is that the processing speed and performance improves. The processor or the device decides the frequency for the task and sets a threshold with room for improvement in the frequency required.

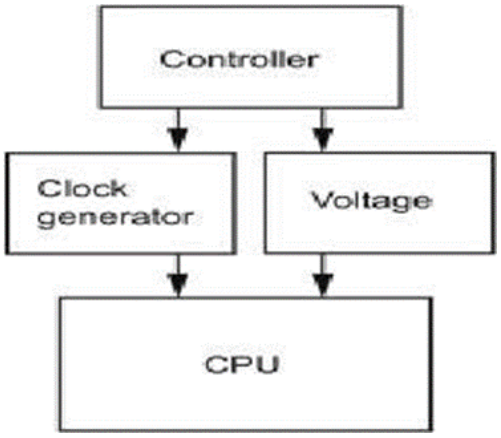

Fig. 6: Dynamic Voltage and frequency scaling

3. Clock gating

The clock gating is an approach by which, the power dissipation in the circuit can be controlled by reducing the frequency of blocks, which is being activated less or disabling them. This technique also helps out reducing the unwanted switching activities and thereby helps out in power saving. The clock gating is done at the architecture level.

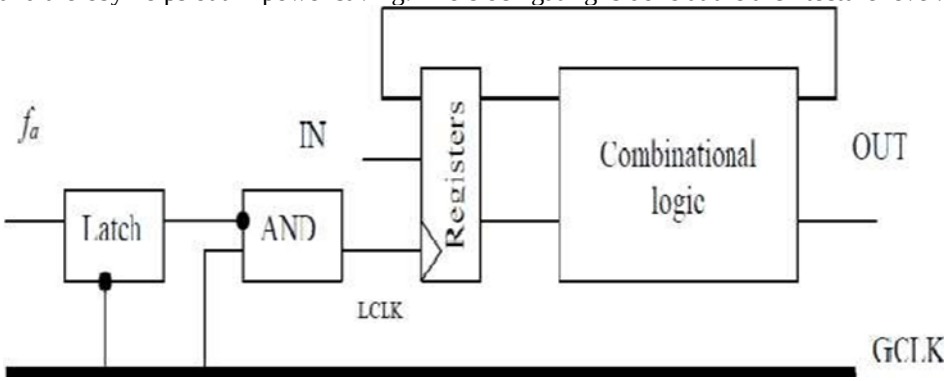

Fig. 7: Clock Gating

VI. CONCLUSION

This paper discusses about the power dissipation and the ways by which low power circuits can be designed at logic and architectural level have been discussed. Power dissipation is one of the major challenges designers are finding difficult to deal with and there has been constant evolution. The paper helps the reader understand the basics of power dissipation and how it is being dealt with in the industry.

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